What is Claimed is:

1. Electrically-programmable integrated circuit antifuse circuitry formed from a semiconductor, comprising:

a metal-oxide-semiconductor antifuse transistor having a drain, source, gate, and substrate, wherein the drain and substrate form a drain-substrate p-n junction in the semiconductor; and

circuitry connected to the antifuse transistor that applies a voltage to the drain that causes avalanche breakdown of the drain-substrate p-n junction and a rise in voltage at the substrate that turns the antifuse transistor on and produces sufficient current between the drain and source to melt the semiconductor and program the antifuse.

2. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 wherein the gate has only a single polysilicon layer.

3. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 further comprising sensing circuitry that senses whether the antifuse transistor has been programmed and outputs a high or low logic signal accordingly.

4. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1, wherein the antifuse transistor is used on an integrated circuit having a core power supply voltage V_{CC}, the electrically-programmable integrated circuit antifuse

transistor further comprising a charge pump that produces a programming supply voltage having a magnitude greater than V_{CC}.

5. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 further comprising a resistor connected between the substrate and a ground.

6. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 further comprising a region of metal that electrically interconnects the gate and the source.

7. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 further comprising a resistor connected between the drain and a positive power supply voltage.

8. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 wherein the gate is electrically connected to the source, the integrated circuit antifuse circuitry further comprising:

a resistor connected between the drain and a positive power supply voltage; and

a second resistor connected between the substrate and a ground potential.

9. The electrically-programmable integrated circuit antifuse circuitry defined in claim 1 wherein

the drain, source, and substrate are surrounded by an n-well isolation region.

10. Electrically-programmable integrated circuit antifuse circuitry formed from a semiconductor, comprising:

a metal-oxide-semiconductor antifuse transistor having a drain, source, gate, and substrate;

at least one Zener diode connected between the drain and substrate; and

circuitry connected to the antifuse transistor and Zener diode that applies a voltage to the drain which causes Zener breakdown of the Zener diode and a rise in voltage at the substrate that turns the antifuse transistor on and produces sufficient current between the drain and source to melt the semiconductor and program the antifuse.

11. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 wherein there are only two Zener diodes connected between the drain and substrate, wherein the two Zener diodes are connected in series.

12. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 wherein the circuitry is formed on an integrated circuit having I/O circuitry powered by an I/O power supply voltage, wherein the voltage applied to the drain that causes the Zener breakdown is the same as the I/O power supply voltage.

13. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 further comprising sensing circuitry that senses whether the antifuse transistor has been programmed and outputs a high or low logic signal accordingly.

14. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 further comprising a resistor connected between the substrate and a ground potential, wherein current through the Zener diode during Zener breakdown passes through the resistor and biases the substrate.

15. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 further comprising a region of metal that electrically interconnects the gate and the source.

16. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 further comprising a resistor connected between the drain and a positive power supply voltage.

17. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 wherein the gate is electrically connected to the source, the integrated circuit antifuse circuitry further comprising:

a resistor connected between the drain and a positive voltage; and

a second resistor connected between the substrate and a ground potential.

18. The electrically-programmable integrated circuit antifuse circuitry defined in claim 10 wherein the drain, source, and substrate are surrounded by an n-well isolation region.

19. A method of programming a metal-oxide-semiconductor integrated circuit antifuse transistor that is formed from a semiconductor and that has drain, source, gate, and substrate regions, and a substrate-source p-n junction, comprising:

raising the voltage of the substrate region relative to the source region to forward bias the substrate-source p-n junction, wherein forward biasing the substrate-source p-n junction injects carriers into the substrate region and turns a parasitic bipolar transistor in the antifuse transistor on, causing current to flow between the drain and source regions that melts the semiconductor and programs the antifuse transistor.

20. The method defined in claim 19 wherein a resistor is connected to the substrate region, and wherein raising the voltage of the substrate region relative to the source region comprises causing current to flow through the resistor to bias the substrate region.

21. The method defined in claim 20 wherein

causing the current to flow through the resistor comprises reverse biasing at least one Zener diode to cause Zener breakdown.

22. The method defined in claim 20 wherein the drain region and substrate region form a drain-substrate p-n junction, and wherein causing the current to flow through the resistor comprises inducing avalanche breakdown in the drain-substrate junction and current flow from the substrate region through the resistor.

23. The method defined in claim 19 wherein the integrated circuit antifuse circuitry is formed on an integrated circuit having I/O circuitry powered by an I/O power supply voltage, the method comprising applying a voltage to the drain during programming at the I/O power supply voltage.